Free Sample Preview

Low-k Dielectric Materials & Process

ILD porosity, integration & CMP

This is a free preview page.

Full version includes more chapters & cases.

Low–k Dielectric Materials & Process

What is low–k?

Dielectrics with k<3.9 reduce RC delay vs. SiO2 (k~3.9); porous low–k (k 2.5–2.9) cuts capacitance further.

Why is it needed?

Interconnect delay, crosstalk & power dominate at advanced nodes (<130nm); key for speed & signal integrity.

Integration challenges

Mechanical weakness, moisture uptake, Cu diffusion barrier; etch / ash / CMP compatibility.

CMP synergy

Soft pads & low down–force avoid delamination; planarizing fragile porous films is the key bottleneck.

Full version: material taxonomy, integration flow, defect modes & characterization methods.